REMARKS

Claims 1-21 were pending. Claims 1, 2, 4-9, 13, 14, and 17-20 have been amended. Reexamination and reconsideration of the present application is respectfully requested.

At the outset, the Examiner is thanked for the thorough review and consideration of the present application. The Examiner's Office Action dated August 5, 2003 has been received and the contents carefully noted.

The Examiner should note that several of the claims, including claims 4-9, 13, 19 and 20, have been amended to correct minor grammatical errors and not in response to any of the Examiner's outstanding rejections.

In the Office Action, the Examiner made a requirement for a substitute specification pursuant to 37 CFR 1.125(a) because of lack of clarity and grammatical errors. Applicants have thoroughly reviewed the specification and have instead amended the specification in the present Amendment to correct unclear sentence structure and grammatical errors and to otherwise place the application in proper idiomatic format. No new matter has been added. Applicants assert that the above amendments adequately and fully address the Examiner's grammatical concerns noted in the Amendment, and therefore respectfully request withdrawal of the objection.

The Examiner rejected claims 1, 2, and 8-17 under 35 USC 112, second paragraph as being indefinite.

Regarding claim 1, Applicants have amended the claim to recite *inter alia*:

an overcurrent protection circuit for decreasing the main current at a first slope and then reducing the main current at a second slope steeper than said first slope, when said main current ~~becomes a first overcurrent that~~ exceeds a predetermined current value for a first period of time equal to or longer than a predetermined period of time; and

an overcurrent limiting circuit for instantaneously dropping the voltage applied to said gate terminal when said main current becomes ~~a second overcurrent~~ larger than said ~~first overcurrent~~ predetermined current value within a second period of time shorter than said predetermined period of time.

Regarding, claim 2, Applicants have amended the claim to recite

wherein said overcurrent limiting circuit decreases the voltage applied to said gate terminal when said main current ~~reaches said second overcurrent~~ becomes larger than said predetermined current value within a third period of time shorter than a delay time defined by said overcurrent protection circuit.

Regarding claims 12 and 13, Applicants submit that the terminology {100} is widely used in the art to express a 3-D crystallographic orientation of an element relative to a plane. For example, such terminology is used in the semiconductor art as recited for example in claim 7 of US Patent No. 6,541,297 which reads: "...wherein the light emitting element and/or the light receiving element and the optical waveguide element are formed on a substrate having planes selected from planes tilted from (100) plane in an A direction (a [011] direction) by an angle in a range of 0 to 55° and planes crystallographically equivalent to such planes..."

The designation {100} is recited in claims 12 and 13 to express the crystallographic representation of the elements that form channels in claim 11. The designation {100} is not meant to be a reference number for any of the drawings.

Regarding claims 8-17, Applicants assume that these claims were rejected as being dependent on claim 1. Claims 8, 9, and 13 have been amended to correct minor

informalities. Claims 14 and 17 have been amended into independent form as they have been found to contain allowable subject matter. Applicants respectfully submit that all of the claims comply with 35 USC 112, second paragraph and request that the Examiner's rejection be withdrawn.

The Examiner rejected claims 18-21 under 35 USC 102(b) as being anticipated by Fukunaga et al. This rejection is respectfully traversed.

Claim 18 has been amended to depend from claim 3, which was found to be allowable. Claims 19-21 depend directly or indirectly from claim 18. Applicants submit that the rejection is now moot in view of the change in dependency and respectfully request that the rejection under 35 USC 102(b) be withdrawn.

The Examiner rejected claims 1, 2, and 9 under 35 USC 103(a) as being unpatentable over Schmidt et al. (US Patent No. 5,550,702) in view of Sasagawa et al. (US Patent No. 5,200,879) and further in view of Masanek et al. (US Patent No. 5,831,807). This rejection is respectfully traversed.

Claim 1 is allowable at least for the reason that claim 1 recites a combination of elements, including for example,

> an overcurrent protection circuit for decreasing the main current at a first slope and then reducing the main current at a second slope steeper than said first slope, when said main current ~~becomes a first overcurrent that~~ exceeds a predetermined current value for a first period of time equal to or longer than a predetermined period of time; and
>
> an overcurrent limiting circuit for instantaneously dropping the voltage applied to said gate terminal when said main current becomes ~~a second overcurrent~~ larger than said ~~first overcurrent~~ predetermined current value within a second period of time shorter than said predetermined period of time.

None of the cited references singly or in combination teaches or suggests at least these features of claim 1.

In the present invention, a semiconductor switching element driving circuit includes an overcurrent protection circuit and an overcurrent limiting circuit. The overcurrent limiting circuit instantaneously drops a voltage of a gate terminal of an IGBT when a main IGBT current becomes larger than a predetermined level i1. The overcurrent protection circuit first decreases the main IGBT current at a first inclination when the main IGBT current becomes larger than the other level i2 lower than the i1 and then rapidly reduces the main IGBT current at a steep second inclination when it becomes smaller than another level i3. Consequently, the overcurrent can be prevented from flowing into the semiconductor switching element and a high-speed cutoff of the semiconductor switching element can be conducted. *See* page 6, lines 4-18 of the specification. In addition, a detection resistance switching unit reduces the resistance value of the current detection resistance.

On page 7 of the Office Action, the Examiner stated Schmidt et al. does not disclose decreasing the main current at a first slope and subsequently at a second slope. The Examiner cites Sasagawa et al. in an attempt to cure the deficiencies of Schmidt et al.

Sasagawa et al. teaches a drive circuit for a voltage driven type semiconductor device. An overcurrent flowing in the semiconductor device is detected based on a current flowing through a serial circuit (resistor and Zener diode) and the presence/absence of a drive signal fed to the drive circuit from an external control circuit. The Examiner refers to Prior Art Figure 3C for allegedly teaching the first and second slopes and the main current value relative to the other overcurrent values.

Column 2, lines 47-57 of Sasagawa et al. reads:

> "In the course of this, the gate-to-emitter voltage V_{GE} of the IGBT Q1 declines with time in accordance with the voltage on the capacitor C2, which is different from the normal turn-off operation as indicated by the solid line after time t2 in FIG. 3C. As a result, the reduction rate of the collector current Ic becomes small, thereby preventing a spike voltage V_{CEP} in the voltage V_{CE} during the current interruption. Incidentally, broken lines in FIG. 3C represent waveforms when an overcurrent is cut off by directly adding the off-gate voltage V2 to the gate of IGBT Q1."

On page 8 of the Office Action, the Examiner states that it would have been obvious to modify Schmidt et al. by "adding a soft cut off of" Sasagawa et al. and that Masanek et al. teaches that "fast, short circuit, protections are necessary to ensure reliable IGBT control of the load."

However, the combination of references fails to disclose the features recited in claim 1, namely, an overcurrent protection circuit for decreasing/reducing the main current in two steps (first slope/inclination and second slope/inclination) and an overcurrent limiting circuit for instantaneously dropping the voltage applied to a gate terminal, to achieve the novel and nonobvious advantages discussed in the present invention.

On page 12 of the Office Action, the Examiner's reasons for allowance state that although Sasagawa et al. disclose decreasing the main current in two steps, the reference does not disclose "a condition for that change in steepness, namely that the main current becomes smaller than a third comparison current that is lower than the second comparison current." The Examiner interpreted the "condition" in claim 1 to be "when said main current becomes a second overcurrent, which exceeds a second predetermined value." Applicants respectfully submit that the Examiner's interpretation is incorrect.

Applicants submit that claim 1, similar to allowed claim 3 recites a "condition for that change in steepness." The "condition" is

> "an overcurrent protection circuit...when said main current exceeds a predetermined current value for a first period of time equal to or longer than a predetermined period of time; and ...an overcurrent limiting circuit...when said main current becomes larger than said predetermined current value within a second period of time shorter than said predetermined period of time."

The combination of references also fails to teach or suggest these features. Instead, in Fig. 3C of Sasagawa et al. the current Ic only appears to be reduced/decreased once at t2. In Masanek et al., an error signal from either window comparator interrupts operation of the power semiconductor component and locks out all higher level control signals to the power semiconductor component.

It can thus be understood that the combination of references does not in any way make obvious the essential features of the present invention as set out in independent claim 1.

Moreover, as claims 2 and 9 depend from independent claim 1, these claims are also allowable for the same reasons as their respective base claim.

Therefore, Applicants respectfully request that the rejection of claims 1, 2, and 9 under 35 USC 103(a) be withdrawn.

The Examiner rejected claim 8 under 35 USC 103(a) as being unpatentable over Schmidt et al. in view of Sasagawa et al., and Masanek et al. and further in view of Fukunaga et al. (US Patent No. 5,375,029). This rejection is respectfully traversed.

The Examiner states that the combination of references fails to teach the features of claim 8 and cites Fukunaga et al. in an attempt to cure the deficiencies of the other three references.

None of the cited references singly or in combination teaches or suggests the features of claim 1, namely, an overcurrent protection circuit for decreasing/reducing the main current in two steps (first slope/inclination and second slope/inclination) and an overcurrent limiting circuit for instantaneously dropping the voltage applied to a gate terminal, to achieve the novel and nonobvious advantages discussed in the present invention. Claim 8 depends from claim 1 and is allowable at least for the same reasons as claim 1.

Fukanaga et al. teaches an overcurrent protection circuit of a power device and a semiconductor integrated circuit device. The current Ic is under the overcurrent level OI at curves a and b in Figure 2. It does not appear that the current Ic reduces/decreases in the manner recited in claim 1. Thus, Fukanaga et al. fails to cure the deficiencies of the other three references.

It can thus be understood that the combination of references does not in any way make obvious the essential features of the present invention as set out in independent claim 1.

Therefore, Applicants respectfully request that the rejection of claim 8 under 35 USC 103(a) be withdrawn.

The Examiner rejected claim 10 under 35 USC 103(a) as being unpatentable over Schmidt et al. in view of Sasagawa et al. and Masanek et al. and further in view of Tomomatsu et al. (US Patent No. 5,729,032). This rejection is respectfully traversed.

The Examiner states that the combination of references fails to teach the features of claim 10 and cites Tomomatsu et al. in an attempt to cure the deficiencies of the other three references.

None of the cited references singly or in combination teaches or suggests the features of claim 1, namely, an overcurrent protection circuit for decreasing/reducing the main current in two steps (first slope/inclination and second slope/inclination) and an overcurrent limiting circuit for instantaneously dropping the voltage applied to a gate terminal, to achieve the novel and nonobvious advantages discussed in the present invention. Claim 10 depends from claim 9, which depends from claim 1 and is allowable at least for the same reasons as claim 1.

Tomomatsu et al. teaches a field effect type semiconductor device and manufacturing method wherein the rise of the main current Is of the sensing circuit is delayed from the main current Im of the main circuit to prevent a surge current. The current Is has a value always lower than that of the current Im. It does not appear that either of the currents Is or Im reduce/decrease in the manner recited in claim 1. Thus, Tomomatsu et al. fails to cure the deficiencies of the other three references.

It can thus be understood that the combination of references does not in any way make obvious the essential features of the present invention as set out in independent claim 1.

Therefore, Applicants respectfully request that the rejection of claim 10 under 35 USC 103(a) be withdrawn.

The Examiner rejected claims 11 and 13 under 35 USC 103(a) as being unpatentable over Schmidt et al. in view of Sasagawa et al. and Masanek et al. and further in view of Seok (US Patent No. 5,753,942). This rejection is respectfully traversed.

The Examiner states that the combination of references fails to teach the features of claims 11 and 13 and cites Seok in an attempt to cure the deficiencies of the other three references.

None of the cited references singly or in combination teaches or suggests the features of claim 1, namely, an overcurrent protection circuit for decreasing/reducing the main current in two steps (first slope/inclination and second slope/inclination) and an overcurrent limiting circuit for instantaneously dropping the voltage applied to a gate terminal, to achieve the novel and nonobvious advantages discussed in the present invention. Claim 11 depends from claim 9, which depends from claim 1, claim 13 depends from claim 12, which depends from claim 11 and are allowable at least for the same reasons as claim 1.

Seok teaches power semiconductor devices having arcuate-shaped source regions for inhibiting parasitic thyristor latch-up. The use of arcuate-shaped source regions 7 limits the likelihood of parasitic thyristor latch-up by "spreading" the hole current entering each base region 4 during forward conduction. *See* column 6, lines 14-37. The reference fails to discuss overcurrent protection. Thus, Seok fails to cure the deficiencies of the other three references.

It can thus be understood that the combination of references does not in any way make obvious the essential features of the present invention as set out in independent claim 1.

Therefore, Applicants respectfully request that the rejection of claims 11 and 13 under 35 USC 103(a) be withdrawn.

The Examiner rejected claim 16 under 35 USC 103(a) as being unpatentable over Schmidt et al. in view of Sasagawa et al. and Masanek et al. and further in view of Zeller (US Patent No. 5,550,444). This rejection is respectfully traversed.

The Examiner states that the combination of references fails to teach the features of claim 16 and cites Zeller in an attempt to cure the deficiencies of the other three references.

None of the cited references singly or in combination teaches or suggests the features of claim 1, namely, an overcurrent protection circuit for decreasing/reducing the main current in two steps (first slope/inclination and second slope/inclination) and an overcurrent limiting circuit for instantaneously dropping the voltage applied to a gate terminal, to achieve the novel and nonobvious advantages discussed in the present invention. Claim 16 depends from claim 1 and is allowable at least for the same reasons as claim 1.

Zeller teaches a device and process for the reversible storage of electric energy by its reversible conversion to kinetic energy. In a device with pick-ups, the instantaneous voltage between one phase conductor each and a neutral conductor or another phase conductor of the alternating power supply, the instantaneous voltage between the two terminals of at least one pair of terminals, and also the instantaneous current in one winding each are repeatedly sampled. The reference fails to discuss overcurrent protection. Thus, Zeller fails to cure the deficiencies of the other three references.

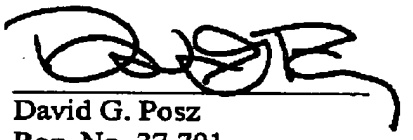
It can thus be understood that the combination of references does not in any way make obvious the essential features of the present invention as set out in independent claim 1.

Therefore, Applicants respectfully request that th rejection of claim 16 under 35 USC 103(a) be withdrawn.

Applicants wish to thank the Examiner for the allowance of claims 3-7 and the indicated allowability of claims 14, 15, and 17. Claims 14 and 17 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 15 depends from claim 14 and therefore is now allowable in view of the amendments to claim 14.

In view of the above remarks, the present application is believed to be in condition for allowance. A prompt notice to that effect is respectfully requested. Although no additional fees are believed to be due, permission is hereby given to charge any unforeseen fees to deposit account 50-1147.

Respectfully submitted,



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